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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,680	01/10/2002	Timothy B. Cowles	500792.03	9219

7590 09/18/2002

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EXAMINER

NGUYEN, VAN THU T

ART UNIT PAPER NUMBER

2824

DATE MAILED: 09/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/043,680

Applicant(s)

COWLES ET AL.

Examiner

VanThu Nguyen

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 11-14, 27-29, 36-38, 42 and 43 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11, 12, 14, 27, 28, 36, 37 and 42 is/are rejected.
- 7) ☒ Claim(s) 13, 19, 38 and 43 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 4, 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claim 42 is rejected under 35 U.S.C. 102(e) as being anticipated by Itou (U.S. Patent No. 6,104,641).

Regarding claim 42, Itou discloses method of refreshing a dynamic random access memory ("DRAM") having a full density operating mode (4-value mode) and a reduced density operating mode (2-value mode), the method comprising determining the operating mode of the DRAM (via MLT, see FIG. 8); if the DRAM is determined to be operating in the full density mode, refreshing the DRAM at a first rate (via transfer gate 86, see FIG. 8); and if the DRAM is determined to be operating in the reduced density mode, refreshing the DRAM at a second rate (via transfer gate 87 and frequency diving circuit 88), the second rate being slower than the first rate (see column 7 lines 7-28).

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2824

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 11-12, 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Itou (U.S. Patent No. 6,104,641).

Regarding claim 11, Itou discloses, in FIG. 8, a refresh controller for use in a dynamic random access memory (DRAM) having a full density mode (4-value mode) and a reduced density mode (2-value mode), the refresh controller comprising an oscillator (84 & 85) generating a periodic clock signal (RF); a counter (89) having a clock input terminal couple to receive the clock signal, the counter inherently having first and second stages the first of which increments at a faster rate than the second; and a selector circuit (86, 87 and 88) for *outputting to the counter* a first clock rate (via transfer gate 86) in the full density mode and outputting a second clock rate (via transfer gate 87 and frequency diving circuit 88) in the reduced density mode, wherein first clock rate is faster than the second clock rate (see column 7 lines 7-28).

Even though Itou doesn't disclose that the selector circuit coupled *to receive outputs from the counter*, it would have been obvious to one with ordinary skill in the art to realize that changing order of how the counter and selector circuit being coupled does not effect the circuit operation of the refresh controller.

Regarding claim 12, Itou further discloses the selector circuit comprising a first pass gate (86) and a second pass gate (87); a control circuit (Mode Register 15 for producing MLT signal, see FIG. 1) for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the pass gate in the reduced density mode.

Regarding claim 14, Itou also discloses the reduced density mode is half density mode (2-value mode is half density of 4-value mode).

5. Claims 27-28, 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shore (U.S. Patent No. 6,044,029) in view of Itou.

Regarding claims 27, Shore discloses, in FIG. 2, a dynamic random access memory (DRAM) comprising a array of memory cells arranged in rows and columns; a column address latch (34) structured to store a column address responsive to a column address strobe signal (CAS\*); a column decoder (56) coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto; a row address latch (32) structured to store a row address responsive to a row address strobe signal (RAS\*); a first row decoder (46) coupled to the row address latch to receive the store row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal (E\_EN); a second row decoder (42) coupled to the row address latch to receive the store row address and active respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal (O\_EN); a mode controller (Repair Enable Circuit 36, which has equivalent function as a mode controller) coupled to the row decoders, the mode controller being operable in a full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address (RA0) and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signal in a reduced density mode regardless of the state of the least

significant bit of the row address; a data path (I/O and I/O\*) coupled between the memory array and a data terminal.

However, Shore doesn't disclose the refresh controller as recited in claim 27, lines 23-34, which is similar to refresh controller recited in claim 11.

Itou discloses a refresh controller as applied to prior rejection of claim 11.

Since Shore and Itou are both from the same field of semiconductor, the purpose disclosed by Itou would have been recognized in the pertinent art of Shore.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art employ the refresh controller disclosed in Itou for the purpose of refreshing the DRAM memory disclosed in Shore in different modes.

Regarding claim 28, Itou discloses all recited limitation in claim 28, which is similar to claim 12 as applied in prior rejection.

Regarding claims 36-37, Shore in view of Itou disclose, as applied in prior rejection of claims 27-28, all claims subject matter. Shore further discloses, in FIG. 6, a data input device (106); a data output device (108); a processor (112) coupled to the data input and output devices.

***Allowable Subject Matter***

- VTN 6. Claims 13, <sup>29</sup>~~28~~, 38, 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
7. The following is a statement of reasons for the indication of allowance or allowable subject matter:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Itou and Share, taken individually or in combination, do not teach the claimed invention having:

the second stage of the counter is two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage; or  
the second rate is 8 times slower than the first rate.


***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (703) 306-9121. The examiner can normally be reached on Monday-Thursday, 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VTN  
September 12, 2002



VanThu Nguyen  
PATENT EXAMINER  
ART UNIT 2824